Thermal Cycle Resister of Semi-Conductive Coating consideration for Step Coverage and On-orbit test

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1. Background and Purpose

Manmade satellites has been supporting our life in many sections now a day. However, these satellites are always exposed to very dangerous space environment and get damaged to normal operations. Recently, faulty operation due to arcing and charging on solar array panel has been confirmed. During the arcing on the solar array panel, there is high possibility of serious problem, which decreases the power generation of solar the leading to stop operation of satellite. Therefore, demand for effective and inexpensive mitigation technology is increasing. It has been reported that potential difference between the satellite chassis and insulating coverglass is the origin of an arc. Therefore, we consider reducing the potential difference by using the semi-conductive coating on the solar cell coverglass that ultimately prevent the arc. Therefore, the purpose of this research is to mitigate the arcing and charging by semi-conductive coating.

2. Semi-conductive coating

Semi-conducive coating liquid is consisted of silica (base material) and ATO (Antimony Tin Oxide) corpus. ATO is spread on the base material. This coating liquid can change optional surface resistivity. It is adjusted to 10^8 Ω/sq. The merit of this research is as follows:.

1. To be able to coat a whole surface.
2. To reduce a cost and workload than former charging mitigation method.

But, this research has several problems. First, generation power of solar array reduces due to whole surface coating. This reason is that transmittance of sunlight is degraded from several percent due to semi-conductive layer. Although thin coating can increase the sunlight transmittance, the coating around the edge or step is not satisfactory. In this case, we made semi-conductive liquid of different coefficient of viscosity. And we use two liquids of different viscosity on the whole surface and edge. This way we tried to improve an optical transparency. Secondly, semi-conductive layer is not durable to space environment. Space environment is consisted of radiation, Ultra-Violate and thermal cycle etc. Semi-conductive layer is similar to glass as so to be an inorganic compound after heating. So, we think that semi-conductive layer is weak to sharp change in temperature, and conducted the thermal cycle test.

3. Thermal cycle test

Thermal cycle test was conducted in atmosphere inside a thermostatic chamber. Figure1 shows the test sample, that is, coated solar cells. We prepared two samples, sample1 (whole surface coat:3, edge coat:4) and sample2 (whole surface coat:4, edge coat:9). Generation power decreasing rate of these samples was about 10%. Thermal cycle test condition is shown below.

Max temparature:100℃, Min temperature:-150℃, Baking time:0 min, Cycle time:50 min

Max and Min temperature is simulated geostationary orbit. Cycle number was 5cycle, 10cycle and 100cycle.

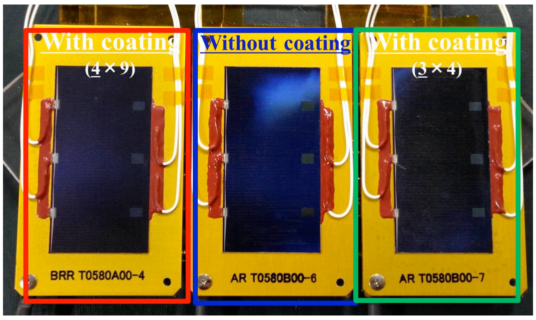

Figure 1, Test sample

Table1 shows the result after the surface is exposed to 7keV electron beam. Arc was not occurred on the coated sample. On other condition, they showed the same results. Figure 2 shows the potential distribution of coated and non-coated samples after being exposed to electron beam. Coated sample shows no differential potential has been developed unlike the non-coated sample. Therefore, we confirmed the charging mitigation due to coating. In addition, we think that semi-conductive layer is able to endure the thermal cycles.

Table 1 Arcing number of each samples after thermal cycle

	With coating (4×9)	**With coating (3×4)**	**Without coating**
5 cycle	0	0	1
10 cycle	0	0	6
100 cycle	0	0	11

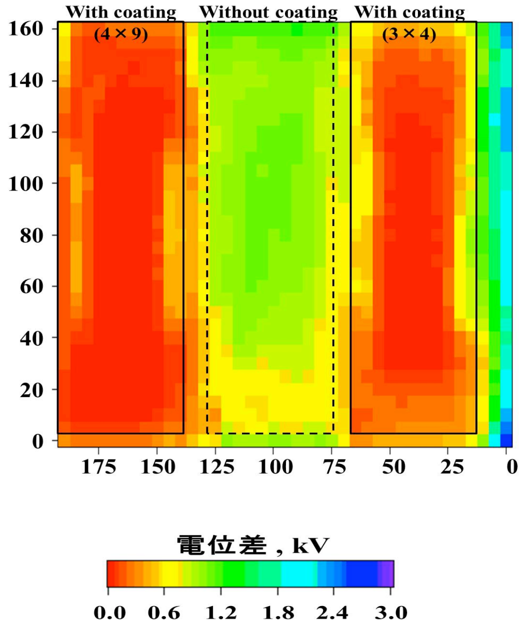

Figure 2 Surface potential distribution.

(Case of irradiating 7keV electron for sample after 100 thermal cycle)

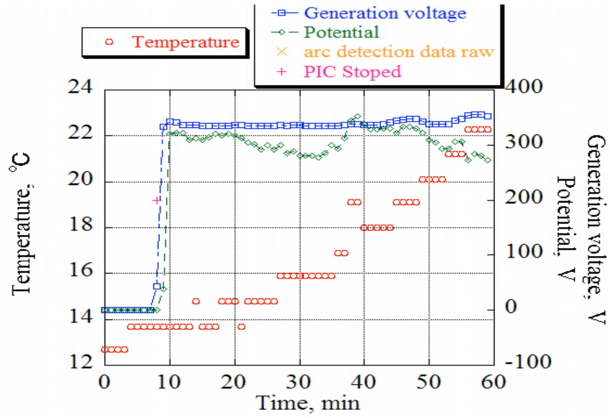

Figure3 On-orbit high voltage generation for arcing test

Table2 Summary of on-orbit test result.

	Without coating	With coating
Test time, min	678	650
Arcing number	17	0

4. On-orbit test

This technology was equipped with high voltage demonstration satellite “HORYU-II”, launched from Tanegashima space center on May 18, 2012. This satellite could make an arcing environment to satisfy this purpose. We conducted the arcing mitigation test by coating under the arcing environment. Generation power of coating solar cells decreased 34% because of thickly painting. We verified not only arcing mitigation but also durability of semi-conductive layer.

Fifure3 shows result of on-orbit test. Arc did not occurred but we made an arcing environment on purpose. Table2 shows arcing number of each solar array. From table2, we confirm that arc never occurred on coating solar array. Semi-conductive layer could demonstrate that it is able to endure to space environment for 182 days. So, we confirm that thermal cycle is not able to destroy the semi-conductive layer exposed to 2548 cycle (14 cycle/day × 182 days).

5. Conclusion and Future task

We conducted the thermal cycle test at coating solar array, using two coating liquid of different viscosity. Degradation rate of generation power is about 10%, and these samples were not prone to arc after thermal cycle exposure. In addition, semi-conductive coating can also be applied for arcing mitigation confirmed by high voltage technology demonstration satellite ‘HORYU-II’.

As future task, we like to conduct the following verification test and improvement.

①Space environment resistance will be confirmed by exposing to UV irradiation and atomic oxygen.

②Improvement of coating wettability for several material (such as polyimide, RTV, etc.)

③New functionality imparting to coating liquid

We think that semi-conductive coating can make rapid progress by coating improvement and verification test.